AN3334
Application note

SPC560P50/SPC56AP60 HW/SW comparison

Introduction

This document addresses HW/SW differences between two 32-bit system-on-chip (SoC) automotive microcontrollers of the SPC56xP family: SPC560P50 and SPC56AP60 devices.

When designing a system using an SPC560P50 device, HW/SW differences must be considered for a subsequent and eventual migration to an SPC56AP60 device.

All topics covered in this document refer to *RM0022,* Rev. 3 (see *A.1: Reference document* in *Appendix A*).

This application note applies to the SPC560P50/SPC56AP60 devices listed in *Table 1*.

Table 1. Device summary

Part number	Package
SPC560P50L3	LQFP100
SPC560P50L5	LQFP144
SPC56AP60L3	LQFP100
SPC56AP60L5	LQFP144

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1 SPC560P50/SPC56AP60 device comparison

Table 2. SPC560P50/SPC56AP60 device comparison(1) (2)

Feature	SPC560P50	SPC56AP60
Core	Single-core e200z0h	Dual-core e200z0h
System clock	Up to 64 MHz	
Code Flash memory (with ECC)	512 Kbyte	1024 Kbyte(3)
Data Flash memory / EE (with ECC)	4 × (16 Kbyte)	4 × (16 Kbyte)
SRAM (with ECC)	40 Kbyte	80 Kbyte
FlexCAN (controller area network)	2 × (32 MB)	3 × (32 MB)
Safety port	Yes (via second FlexCAN module)	
LINFlex	2 × (2 × M/S)	
DSPI (deserial serial peripheral interface)	4 × (up to 8/4/4/4 CS)	5 × (up to 8/8/4/4/4 CS)(4)
eTimer	2 × (2 × 6 channels)	
ADC (analog-to-digital converters)	2 × 10-bit	1 × 10-bit(5)
FlexPWM (pulse-width modulation)	1 × (4 × 2 channels)	No
CTU (cross triggering unit)	1 × (8 events)	1 × (8 events)(6)
FlexRay	1 × (32 MB)	1 × (64 MB)
FMPLL (frequency-modulated phase locked loop)	2	1
IRC OSC (16 MHz)	1	
External interrupts	32	
eDMA (enhanced direct memory access)	1 × (16 channels)	
FCU (fault collection unit)	Yes	Yes(7)
CRC (cyclic redundancy check) unit	1	2(8)
Junction temperature sensor	Yes	No
Debug port	JTAG; Nexus class 2+	JTAG; Nexus class 2+(9)
Supply voltage	3.3 V or 5 V single supply with external ballast transistor	
Packages	LQFP100, LQFP144	LQFP100, LQFP144, LQFP176(10)
Temperature range	–40 to 125 °C	

1. The comparison is made between two different devices both in “Full Featured” configuration.
2. Acronyms used: *MB* = message buffer, *M/S* = master/slave, *CS* = chip select
3. Dual port Flash Controller with 4 buffers per port and support for pre-fetching
4. Increased number of CSs for DSPI_1
5. With pre-sampling capability
6. With ADC commands remapping
7. Enhanced FCCU version
8. Upgraded specification with addition of 8-bits polynom (CRC-8) support and 3rd context

9. Improved debugging capability with data trace capability and increased Nexus throughput available on emulation package
10. Emulation package only. Not available for production

2 Device pinout and pin multiplexing

Pinout compatibility is very important when designing hardware destined to support multiple devices within one product family. For this reason, the SPC56AP60 pin multiplexing is based on that of the SPC560P50 to ensure the pinouts of both devices are fully compatible.

Table 3 shows the SPC560P50 functions which have been added to the pin multiplexing of the SPC56AP60 device. *Table 4* shows ADC_0 channel functions on SPC56AP60 that are functions of ADC_1 on the SPC560P50 device.

Moreover the pin multiplexing FlexPWM_0 functions are removed on the SPC56AP60 and the FCCU I/Os replace the SPC560P50 FCU I/Os.

Furthermore the following device enhancements found on the SPC56AP60 need to be taken into account as they require an adaptation of the external pull-up/down resistor circuit on two specific pins:

- BCTRL pin:
  - SPC560P50: An external pull-down resistor must be implemented
  - SPC56AP60: A pull-down resistor is integrated, thus BCTRL pin is not connected (the same for SPC560P40xx devices).
- RESET pin:
  - SPC560P50: is pulled-up
  - SPC56AP60: is internally pulled-down increasing the device safety

Table 3. SPC56AP60 pin multiplexing: added functions

Port pin	Alternate function	Function	Peripheral
A[2]	ALT2	CS3	DSPI_4
A[6]	ALT2	CS2	DSPI_4
A[7]	ALT2	CS1	DSPI_4
A[8]	ALT2	CS0	DSPI_4
A[9]	ALT2	SIN	DSPI_4
B[2]	ALT2	SOUT	DSPI_4
B[3]	ALT2	SCK	DSPI_4
C[5]	ALT2	SCK	DSPI_4
C[7]	ALT2	SIN	DSPI_4
C[8]	ALT2	CS1	DSPI_4
C[9]	ALT2	CS0	DSPI_4
C[10]	ALT2	CS2	DSPI_4
D[6]	ALT3	SOUT	DSPI_4
G[2]	ALT2	SIN	DSPI_4
G[3]	ALT2	SOUT	DSPI_4
G[4]	ALT2	SCK	DSPI_4
G[5]	ALT2	CS0	DSPI_4

Table 3. SPC56AP60 pin multiplexing: added functions (continued)

Port pin	Alternate function	Function	Peripheral
G[6]	ALT2	CS1	DSPI_4
G[7]	ALT2	CS2	DSPI_4
G[8]	ALT2	CS3	DSPI_4
A[13]	ALT1	CS4	DSPI_1
A[14]	ALT3	CS5	DSPI_1
A[15]	ALT1	CS6	DSPI_1
B[1]	ALT1	CS7	DSPI_1
D[1]	ALT1	CS4	DSPI_1
D[2]	ALT1	CS5	DSPI_1
D[9]	ALT3	CS6	DSPI_1
D[12]	ALT3	CS7	DSPI_1
G[5]	ALT2	CS4	DSPI_1
G[6]	ALT2	CS5	DSPI_1
G[7]	ALT2	CS6	DSPI_1
G[8]	ALT2	CS7	DSPI_1
D[8]	ALT2	RDY	Nexus
G[12](1)	ALT1	RDY	Nexus
C[13]	ALT3	RX	FlexCAN_1
C[14]	ALT3	TX	FlexCAN_1
G[9]	ALT2	RX	FlexCAN_1
G[10]	ALT2	TX	FlexCAN_1

1. This port pin is not present on SPC560P50

Table 4. SPC56AP60 pin multiplexing: ADC channels

Port pin	Function	Peripheral
B[13]	AN[16]	ADC_0
B[14]	AN[17]	ADC_0
B[15]	AN[18]	ADC_0
C[0]	AN[19]	ADC_0
D[15]	AN[20]	ADC_0
E[0]	AN[21]	ADC_0
E[8]	AN[22]	ADC_0
E[9]	AN[23]	ADC_0
E[10]	AN[24]	ADC_0

Table 4. SPC56AP60 pin multiplexing: ADC channels (continued)

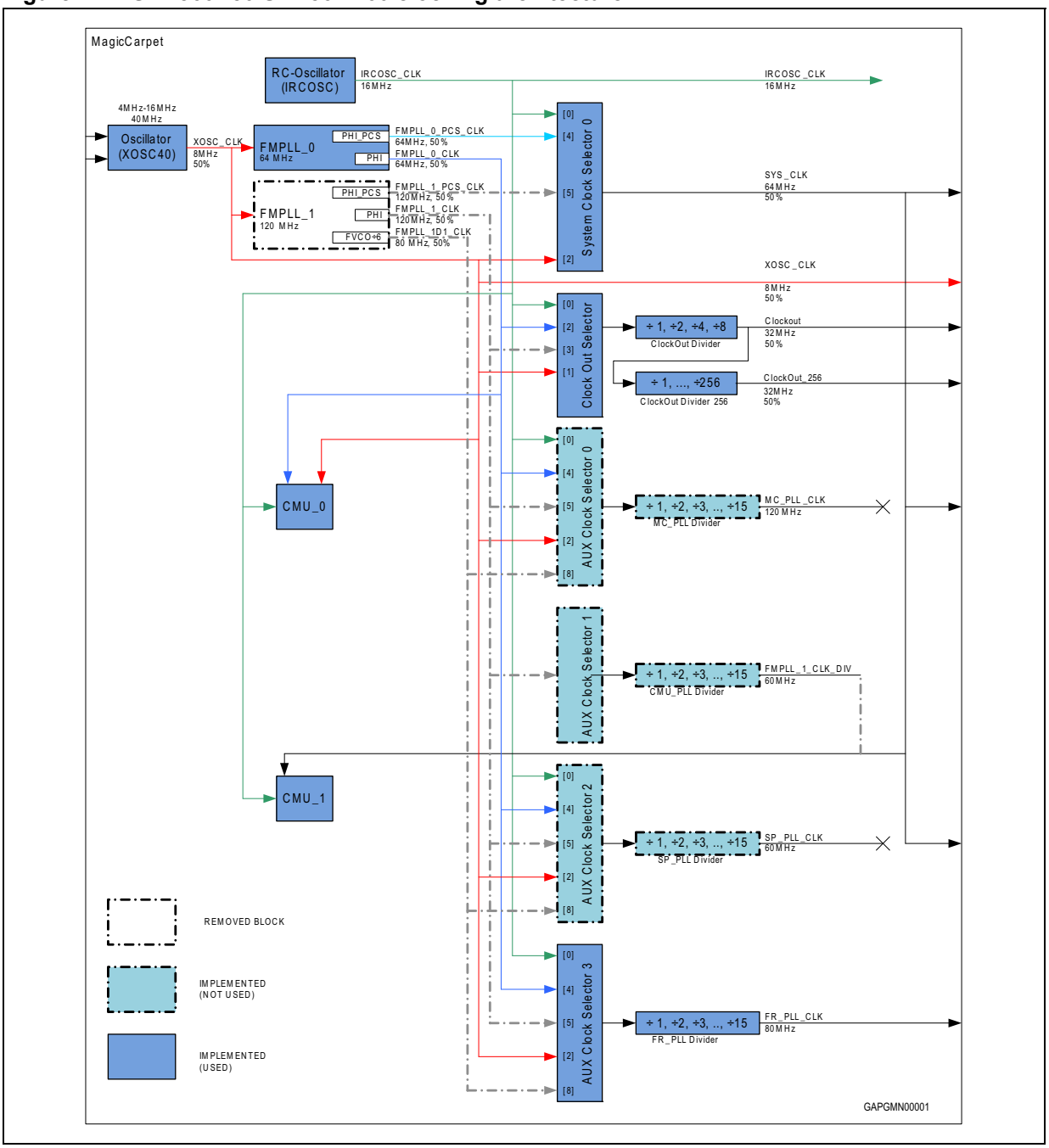
Port pin	Function	Peripheral
E[11]	AN[25]	ADC_0
E[12]	AN[26]	ADC_0

3 Clock distribution and management

The SPC560P50 device implements two PLL sources: FMPLL_0, typically used for system timing, and FMPLL_1, typically used for the timing of the motor control peripherals such as the FlexPWM, CTU, eTimers, and ADC.

On the contrary the SPC56AP60 device has a simplified clock structure: only the FMPLL_0 is available (see *Figure 1*).

Figure 1. SPC560P50/SPC56AP60 clocking architecture



Therefore only FMPLL_0 (or the External Oscillator—XOSC or the Internal RC Oscillator—IRCOSC) can be selected as a source for the device peripherals. This affects the maximum speed of motor control peripherals. The maximum peripheral operating speed is attained when the system clock runs at 64 MHz, whereas on the SPC560P50 device the peripheral clock runs at up to 120 MHz. The maximum speed for peripherals using a motor control clock base can have an impact on external interactions such as the input capture of external signals, PWM output generation and all other timing operations. *Table 5* provides a summary of the maximum device clock speeds.

Table 5. Maximum system clock speed for motor control peripherals

Peripheral	Maximum peripheral clock (MHz)	
	SPC560P50	SPC56AP60
eTimer_0	120	64
eTimer_1	120	64
FlexPWM	120	Not implemented
ADC_0	120	64
ADC_1	120	Not implemeted
CTU	120	64

Note: On the SPC56AP60 device CMU_1 is used to monitor system clock (SYS_CLK) and the output of FMPLL_1 (FMPLL_1_CLK_DIV) on SPC560P50 devices.

4 Flash memory

4.1 Code Flash memory

The SPC56AP60 device code Flash memory is different in size and sectorization than the SPC560P50 device one (see *Table 2*). *Table 6* compares the code Flash memory sectorization of the two Flash memories.

Table 6. SPC560P50/SPC56AP60 code Flash memory sectorization comparison

Start address	End address	Size [KB]	SPC56AP60(1)	SPC560P50(1)	Region
0x00000000	0x00003FFF	16	X	X	Code Flash Array 0
0x00004000	0x00007FFF	16	X		Code Flash Array 0
0x00008000	0x0000BFFF	16	X	X	Code Flash Array 0
0x0000C000	0x0000FFFF	16		X	Code Flash Array 0
0x00010000	0x00013FFF	16	X	X	Code Flash Array 0
0x00014000	0x00017FFF	16			Code Flash Array 0
0x00018000	0x0001BFFF	16	X	X	Code Flash Array 0
0x0001C000	0x0001FFFF	16	X		Code Flash Array 0
0x00020000	0x0002FFFF	64	X	X	Code Flash Array 0
0x00030000	0x0003FFFF	64	X		Code Flash Array 0
0x00040000	0x0005FFFF	128	X	X	Code Flash Array 0
0x00060000	0x0007FFFF	128	X	X	Code Flash Array 0
0x00080000	0x0009FFFF	128	X	O	Code Flash Array 1
0x000A0000	0x000BFFFF	128	X	O	Code Flash Array 1
0x000C0000	0x000DFFFF	128	X	O	Code Flash Array 1
0x000E0000	0x000FFFFF	128	X	O	Code Flash Array 1

1. X = available, O = not available

4.2 Data Flash memory

SPC56AP60 devices utilize the latest version of the data Flash memory (as already implemented on SPC560P40xx). *Table 7* compares the features of the two Flash memories.

Table 7. SPC560P50/SPC56AP60 data Flash memory feature comparison

Features	SPC560P50	SPC56AP60	Comments
Memory size	64 Kbyte + 8 Kbyte test Flash		Identical
Sectorization	4 × 16 Kbyte (B0F0,1,2,3 mapped only to low-address space)		Identical
Memory mapping	4 × 16 Kbyte (B0F0,1,2,3 mapped only to low-address space)		Identical
Access time	40 ns	120 ns	Longer access time
Memory organization	Logical organization = 64 bit Physical organization = 128 bit	Logical organization = 32 bit Physical organization = 32 bit	Different physical organizations
ECC	64-bit and 8-bit ECC	32-bit and 7-bit ECC	Different ECC but identical states to EEPROM emulation
Sector protection	Modify protection against unwanted program, erase		Identical
Data Flash protection against piracy	Protection defined in code Flash memory		Identical
Code Flash disabling in sleep mode	Yes	Not supported Do not use	Difference only if sleep mode is used
Flash interface	—	UT2, UMISR 2,3,4 Not used due to the 32-bit read	—

4.2.1 ECC and EEPROM emulation

The ECC is different when implemented on 32-bit data instead of 64-bit data but the ECC coding has been defined so that the different states used for EEPROM emulation are identical.

Therefore the same states can be used for the EEPROM emulation.

4.2.2 Programming

The programing is changed from 64-bit in SPC560P50 to 32-bit in SPC56AP60. The change can be hidden by a low-level driver if the low-level driver implements the 64-bit programming as two consecutive 32-bit programming operations.

4.2.3 Reading

The longer access time should in theory lead to differences in real-time behavior. As for SPC560P50, the Flash prefetch controller allows to hide all differences provided that:

- The number of wait states is increased (3 × more wait states).
- The Flash prefetch buffer is disabled.

4.2.4 Array integrity check

Once the array integrity check operation is completed, the SPC560P50 data Flash memory driver compares the total content of User Multiple Input Signature Register 0–4 (UMISR0–4) against expected values whereas the SPC56AP60 Data Flash memory driver evaluates the content of only UMISR0–1. The UMISRs contain the results of the read operations, ECC and ECC status.

- SPC560P50
  - UMISR0–3 contain read data 128 bits wide (2 double words)
  - UMISR4 contains 2 × 8-bit ECC and 2 × ECC status (single and double error detection)
- SPC56AP60
  - UMISR0 contains read data 32 bits wide (1 word)
  - UMISR1 contains 1 × 7-bit ECC and ECC status

4.2.5 Margin read

The SPC56AP60 evaluates UMISR0–1 content. Outputs of margin read are checksum values in UMISR0–1. A read reset operation is not used.

The SPC560P50 handles a margin read operation differently using a read reset operation. The results of the margin reads can be checked by comparing them with previously stored expected data. To exit from the margin read mode, a read reset operation must be executed.

4.2.6 ECC logic check

The SPC560P50 data Flash memory driver uses User Test Register 2 (UT2) for odd word input data storage. All UMISR0–4 contents are compared against expected values. UT0.DSI0–7 provides 8-bit data due to the 8-bit ECC calculation.

The SPC56AP60 does not have register UT2, because word access does not need to store odd word of double word value. Only UMISR0–1 contents are evaluated. UT0.DSI0–6 provides 7-bit data due to 7-bit ECC calculation.

Evaluation of only UMISR0–1 is sufficient because of the same reason as described for the array integrity check operation.

4.2.7 Summary

The application overview is summarized in *Table 8*.

Table 8. Application view

Features	SPC560P50/44xF	SPC56AP60xF	Comments
Access time	40 ns	120 ns	Longer access time
Code Flash disabling in sleep mode	Yes	Not supported Do not use	Difference only if sleep mode is used
Flash programming	64-bit	32-bit	Compatible if 2 x 32-bit programming used instead of single 64-bit programming
Sector erase	Same commands		Identical software can be used.
Erase suspend / resume	Same commands		Identical software can be used.
Flash protection modification	Same commands		Identical software can be used.
Flash margin read	Uses read reset commands	No read reset required Use UMISR0–1.	Different API
Array integrity check	—	UMISR 2,3,4 Not used due to the 32-bit read	Same principle but different registers and different signature for same logical content
ECC logic check	—	UT2, UMISR 2,3,4 Not used due to the 32-bit read	Same principle but different registers and different tests and results for ECC logic check
Flash controller	Wait states defined in register		Different PFCR1 register initialization

Most of the differences can be hidden by a low-level driver. The software drivers provided by STMicroelectronics™ for AUTOSAR (AUTomotive Open System ARchitecture) and non-AUTOSAR Flash programming and EE-emulation hide all changes.

When using STMicroelectronics™ Flash drivers and STMicroelectronics™ MCAL (MCU initialization includes Flash prefetch controller configuration) only self-test drivers require changes.

5 Interrupts

SPC56AP60 is a 32-bit dual-core device which implements two interrupt controllers, one for each core. To retain the compatibility with the single-core SPC560P50 device which implements a single interrupt controller, each external interrupt source or peripheral interrupt source—except for the on-platform peripheral sources SEM4_x, ECSM_x, STM_x, and SWT_x—is connected to both interrupt controllers.

5.1 External interrupts

SPC56AP60 device implements the same set of external interrupts available on SPC560P50 device (see *Table 9*).

Table 9. External interrupts

External interrupt sources		SPC560P50(1)	SPC56AP60(1)
EXT_INT[0:7]	GROUP_0	X	X
EXT_INT[8:15]	GROUP_1	X	X
EXT_INT[16:23]	GROUP_2	X	X
EXT_INT[24:31]	GROUP_3	X	X

1. Available

5.2 Peripheral interrupt sources

Interrupt sources and their configuration between SPC560P50 and SPC56AP60 devices is software compatible with the exception due to the missing peripherals on SPC560P50 or SPC56AP60:

- FlexPWM_0, FCU and ADC_1 are missing on SPC56AP60 devices;
- FlexCAN_1, DSPI_4, and FCCU are missing on SPC560P50 devices.

6 eDMA

DMA sources and their configuration are the same on both SPC560P50 and SPC56AP60 devices with the following exceptions (see *Table 10*):

1. The FlexPWM WR source is removed on the SPC56AP60.
2. The DSPI_4 TX source on SPC56AP60 replace the FlexPWM RD source on SPC560P50.
3. The DSPI_4 TX source on SPC56AP60 replace the ADC_1 source on SPC560P50.

Table 10. SPC560P50/SPC56AP60 DMA_MUX mapping comparison

DMA MUX input #	DMA request	
	SPC560P50	SPC56AP60
DMA MUX Source #1	DSPI_0 TX	DSPI_0 TX
DMA MUX Source #2	DSPI_0 RX	DSPI_0 RX
DMA MUX Source #3	DSPI_1 TX	DSPI_1 TX
DMA MUX Source #4	DSPI_1 RX	DSPI_1 RX
DMA MUX Source #5	DSPI_2 TX	DSPI_2 TX
DMA MUX Source #6	DSPI_2 RX	DSPI_2 RX
DMA MUX Source #7	DSPI_3 TX	DSPI_3 TX
DMA MUX Source #8	DSPI_3 RX	DSPI_3 RX
DMA MUX Source #9	CTU	CTU
DMA MUX Source #10	CTU FIFO 1	CTU FIFO 1
DMA MUX Source #11	CTU FIFO 2	CTU FIFO 2
DMA MUX Source #12	CTU FIFO 3	CTU FIFO 3
DMA MUX Source #13	CTU FIFO 4	CTU FIFO 4
DMA MUX Source #14	FlexPWM WR	Removed
DMA MUX Source #15	FlexPWM RD	DSPI_4 TX
DMA MUX Source #16	eTimer_0 CH1	eTimer_0 CH1
DMA MUX Source #17	eTimer_0 CH2	eTimer_0 CH2
DMA MUX Source #18	eTimer_1 CH1	eTimer_1 CH1
DMA MUX Source #19	eTimer_1 CH2	eTimer_1 CH2
DMA MUX Source #20	ADC_0	ADC_0
DMA MUX Source #21	ADC_1	DSPI_4 RX
DMA MUX Source #22	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #23	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #24	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #25	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #26	ALWAYS requestors	ALWAYS requestors

Table 10. SPC560P50/SPC56AP60 DMA_MUX mapping comparison (continued)

DMA MUX input #	DMA request	
	SPC560P50	SPC56AP60
DMA MUX Source #27	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #28	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #29	ALWAYS requestors	ALWAYS requestors
DMA MUX Source #30	ALWAYS requestors	ALWAYS requestors

7 Peripherals

7.1 AIPS

The SPC56AP60 devices are equipped with a new version of AIPS with includes configurable registers for configuring access to peripherals registers (PACR registers for on-platform peripherals and OPACR registers for off-platform peripherals).

7.2 DSPI

The following list summarizes the difference between the SPC560P50 and the SPC56AP60 devices:

- on SPC56AP60 devices, there is one more DSPI (DSPI_4);
- on SPC56AP60 devices, DSPI_1 has 4 more CS;
- on SPC56AP60 devices, user needs to enable each DSPI module (default value is disable) before he can initiate any DSPI operation;
- on SPC56AP60 devices, the DSPI uses the ss_b signal to generate the stop request acknowledge signal (only in slave mode);
- on SPC56AP60 devices, two bits in CMD field of TXPUSH register are used to mask the delays T_{CSC} and T_{ASC} for the selected CTAR in case of Continuous Selection Format.

7.3 LINFlex

On SPC56AP60 the LINFlex registers BDRL and BDRM are also BYTE or HALF WORD accessible while on SPC560P50 devices they are only WORD writable.

7.4 eTimer

As difference in respect to the SPC560P50 devices, a DMA enable bit (default value 0, DMA disabled) was added to the DMA request select registers (DREQ registers) for the IP implemented on SPC56AP60 devices. According to this, on SPC56AP60 devices, it is necessary to set the DMA enable bit to 1 in order to use DMA.

7.5 CRC

As difference in respect to the SPC560P50 devices, SPC56AP60 devices implement an enhaced version of CRC. this enhanced CRC implements 3 contexts and supports a 3rd 8-bits polynom (CRC-8 VDA CAN). Anyway back-compatibility with previous version implemented on SPC560P50 devices is assured.

7.6 FlexPWM

FlexPWM module is not present on all SPC56AP60 devices.

7.7 Junction temperature sensor

Junction temperature sensor is not present on all SPC56AP60 devices.

7.8 ADC

The SPC56AP60 devices implement only one ADC (ADC_0) of 27 channels while the SPC560P50 devices implement two ADC (ADC_0 and ADC_1) of 12 channels each one plus 4 shared channels.

On SPC56AP60 the ADC_0 implements a pre-sampling feature, the pre-sampling voltage is configurable and it can be VSS_HV_ADC or VDD_HV_ADC.

On SPC56AP60 the ADC_0 channel 15 internally connected to the 1.2 V core voltage as on SPC560P50 devices. On SPC560P50 the ADC_1 channel 15 internally connected to the junction temperature sensor which is missing on SPC56AP60 devices.

From a pinout point of view, SPC56AP60 and SPC560P50 devices have the same number of ADC channels on packages LQFP100 and LQFP144 (see *Table 11*).

Table 11. SPC560P50/SPC56AP60 ADC channels comparison

Package	SPC560P50	SPC56AP60
LQFP100	6 ADC_0 channels + 6 ADC_1 channels + 4 ADC_0/1 shared channels	16 ADC_0 channels
LQFP144	11 ADC_0 channels + 11 ADC_1 channels + 4 ADC_0/1 shared channels	26 ADC_0 channels

7.9 CTU

SPC56AP60 devices implement the same CTU implemented on SPC560P50 devices with an additional hardware block placed, as shown in *Figure 2*, between the CTU and the ADC_0 module. This hardware block provides automatic hardware remapping functionality of ADC commands to avoid changes to CTU IP (which can support only 16 channels for each ADC) and to ensure software compatibility for ADC measurement using CTU between SPC560P50 and SPC56AP60 devices. *Table 12* shows how commands for ADC_1 are remapped as command for ADC_0.

Figure 2. CTU/ADC commands remapping IP on SPC56AP60

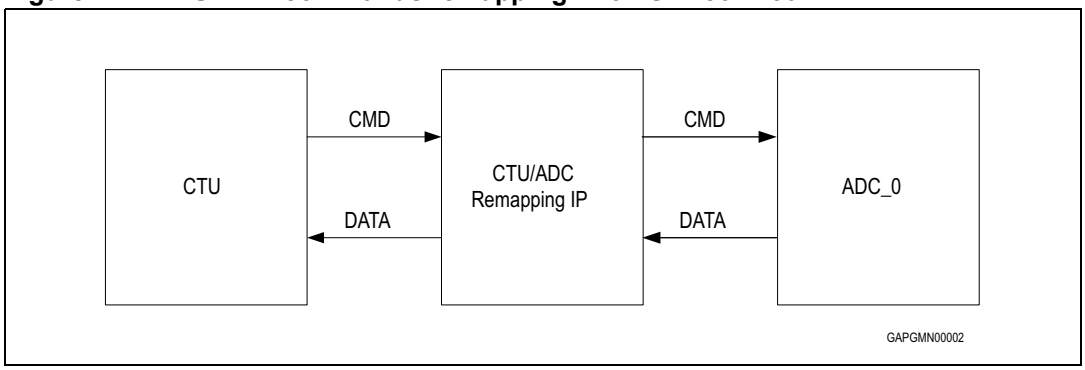


Table 12. CTU/ADC commands remapping IP on SPC56AP60

ADC_0 samples		ADC_1 samples	
Input command	Output command	Input command	Output command
Sample ADC_0 ch[0]	Sample ADC_0 ch[0]	Sample ADC_1 ch[0]	Sample ADC_0 ch[16]
Sample ADC_0 ch[1]	Sample ADC_0 ch[1]	Sample ADC_1 ch[1]	Sample ADC_0 ch[17]
Sample ADC_0 ch[2]	Sample ADC_0 ch[2]	Sample ADC_1 ch[2]	Sample ADC_0 ch[18]
Sample ADC_0 ch[3]	Sample ADC_0 ch[3]	Sample ADC_1 ch[3]	Sample ADC_0 ch[19]
Sample ADC_0 ch[4]	Sample ADC_0 ch[4]	Sample ADC_1 ch[4]	Sample ADC_0 ch[20]
Sample ADC_0 ch[5]	Sample ADC_0 ch[5]	Sample ADC_1 ch[5]	Sample ADC_0 ch[21]
Sample ADC_0 ch[6]	Sample ADC_0 ch[6]	Sample ADC_1 ch[6]	Sample ADC_0 ch[22]
Sample ADC_0 ch[7]	Sample ADC_0 ch[7]	Sample ADC_1 ch[7]	Sample ADC_0 ch[23]
Sample ADC_0 ch[8]	Sample ADC_0 ch[8]	Sample ADC_1 ch[8]	Sample ADC_0 ch[24]
Sample ADC_0 ch[9]	Sample ADC_0 ch[9]	Sample ADC_1 ch[9]	Sample ADC_0 ch[25]
Sample ADC_0 ch[10]	Sample ADC_0 ch[10]	Sample ADC_1 ch[10]	Sample ADC_0 ch[26]
Sample ADC_0 ch[11]	Sample ADC_0 ch[11]	Sample ADC_1 ch[11]	Not valid – force EOC
Sample ADC_0 ch[12]	Sample ADC_0 ch[12]	Sample ADC_1 ch[12]	Not valid – force EOC
Sample ADC_0 ch[13]	Sample ADC_0 ch[13]	Sample ADC_1 ch[13]	Not valid – force EOC
Sample ADC_0 ch[14]	Sample ADC_0 ch[14]	Sample ADC_1 ch[14]	Not valid – force EOC
Sample ADC_0 ch[15]	Sample ADC_0 ch[15]	Sample ADC_1 ch[15]	Not valid – force EOC
Dual sampling ADC_0 ch[x] / ADC_1 ch[y]		Not valid – force EOC	

7.10 SWT

In respect to the SPC560P50 device, the SPC56AP60 features an enhanced version of SWT. This enhanced SWT implements a program flow control monitor with 16-bit pseudorandom key generation servicing sequence. Backward compatibility with the previous SWT version implemented on the SPC560P50 device is ensured.

7.11 SSCM

On SPC560P50 the SSCM_MEMCONFIG register contains the information about the code and data Flash memory sizes while on SPC56AP60 it contains the JTAG part number and minor revision ID.

7.12 FlexRay

The SPC56AP60 device implements the same FlexRay version as that of the SPC560P50 device, but has 64 message buffers instead of 32.

7.13 FCCU

In respect to the SPC560P50 device, the SPC56AP60 implements the FCCU instead of the FCU. The FCCU is basically a new IP based on FCU concept. Even if there are many differences between FCCU and FCU from software viewpoint, the FCCU assures the same functionalities as that of the FCU. *Table 13* provides a summary of differences between the FCCU and FCU connections.

Table 13. FCCU SPC56AP60/FCU SPC560P50 connections comparison

Module	Fault type	FCCU input	FCU input	Comment
CORE_0	Core Checkstop mode entered	CF[0]	HRF0	—
CORE_0	Core reset output	CF[1]	HRF1	—
CORE_1	Core Checkstop mode entered	CF[2]	—	Core_1 is missing on SPC560P50 devices
CORE_1	Core reset output	CF[3]	—	Core_1 is missing on SPC560P50 devices
FLASH	Flash fatal error	CF[4]	HRF7	—
JTAG	JTAG reset (TAP controller)	CF[5]	HRF9	—
FCU	FCU Error	—	SRF0	FCU is missing on SPC56AP60 devices
FCU	FCU Software-triggered Error	—	SRF1	FCU is missing on SPC56AP60 devices
Code Flash	ECC Multi bit error	CF[6]	SRF2	—
Data Flash	ECC Multi bit error	CF[7]	SRF3	—
SRAM	ECC Multi bit error	CF[8]	SRF4	—
SWT_0	Software Watchdog Timer Reset	CF[14]	HRF8	—
SWT_1	Software Watchdog Timer Reset	CF[15]	—	SWT_1 is missing on SPC560P50 devices
ECSM_0	ECC not correctable error	CF[16]	—	Not connected on SPC560P50 devices
ECSM_1	ECC not correctable error	CF[17]	—	ECSM_1 is missing on SPC560P50 devices
SSCM_XFER_ERR	SSCM transfer error	CF[22]	—	Not connected on SPC560P50 devices
FMPLL_0	Loss of lock	NCF[2]	HRF3	—
FMPLL_1	Loss of lock	—	HRF5	FMPLL_1 is missing on SPC56AP60 devices
CMU_0	Loss of XOSC clock	NCF[4]	HRF2	—
CMU_0	FMPLL_0_CLK frequency out of range	NCF[5]	HRF4	—
CMU_1	SYS_CLK frequency out of range	NCF[6]	HRF6	MT_CLK is monitored on SPC560P50 devices and SYS_CLK is monitored on SPC56AP60 devices

Table 13. FCCU SPC56AP60/FCU SPC560P50 connections comparison (continued)

Module	Fault type	FCCU input	FCU input	Comment
ECSM_0	ECC 1-bit error correction notification	NCF[8]	—	Not connected on SPC560P50 devices
ECSM_1	ECC 1-bit error correction notification	NCF[9]	—	ECSM_1 is missing on SPC560P50 devices
CRC_0	CRC Output Check	NCF[10]	—	Enhanced CRC signal, it is not avaialble on SPC560P50 devices
CRC_1	CRC Output Check	NCF[11]	—	Enhanced CRC signal, it is not avaialble on SPC560P50 devices anyway CRC_1 is missing on SPC560P50 devices
PMU	LVD 1.2 digital Fault	NCF[13]	HRF15	—
PMU	LVD 4.5 Fault	NCF[14]	HRF11	—
PMU	LVD 2.7 VREG Fault	NCF[15]	HRF12	—
PMU	LVD 2.7 FLASH Fault	NCF[16]	HRF13	—
PMU	LVD 2.7 I/O Fault	NCF[17]	HRF14	—
MC_ME	Software device reset	NCF[21]	—	Not connected on SPC560P50 devices

8 Reset

Table 14 compares the destructive reset sources of both SPC56AP60 and SPC560P50 devices. *Table 15* compares the functional reset sources of both SPC56AP60 and SPC560P50 devices.

Table 14. SPC560P50/SPC56AP60 destructive reset source mapping comparison

Register bit	Module	SPC56AP60 reset source	SPC560P50 reset source
RGM_Dxx[0]	PMU	LVD 1.2 digital	LVD 1.2 digital
RGM_Dxx[1]		Not implemented	Not implemented
RGM_Dxx[2]	SWT_0	Software Watchdog Timer Reset	Software Watchdog Timer Reset
RGM_Dxx[3]	SWT_1	Software Watchdog Timer Reset	Not implemented
RGM_Dxx[4]	PMU	LVD 2.7 VREG	LVD 2.7 VREG
RGM_Dxx[5]	PMU	LVD 2.7 FLASH	LVD 2.7 FLASH
RGM_Dxx[6]	PMU	LVD 2.7 I/O	LVD 2.7 I/O
RGM_Dxx[7:14]		Not implemented	Not implemented
RGM_Dxx[15]	POR	Device PowerOn-Reset from PMU	Device PowerOn-Reset from PMU

Table 15. SPC560P50/SPC56AP60 functional reset source mapping comparison

Register bit	Module	SPC56AP60 reset source	SPC560P50 reset source
RGM_Fxx[0]	JTAG	JTAG reset (TAP controller)	JTAG reset (TAP controller)
RGM_Fxx[1]	Core_0	Core reset output	Core reset output
	Core_1	Core reset output	Not implemented
RGM_Fxx[2]	MC_ME	Software device reset	Software device reset
RGM_Fxx[3]	Core_0	Core Checkstop mode entered	Core Checkstop mode entered
	Core_1	Core Checkstop mode entered	Not implemented
RGM_Fxx[4]	FMPLL_0	Fail Event (Loss of lock)	Fail Event (Loss of lock)
RGM_Fxx[5]	CMU_0	OLR Event (Loss of XOSC clock)	OLR Event (Loss of XOSC clock)
RGM_Fxx[6]	CMU_0	FHH OR FLL Event (FMPLL_0_CLK frequency out of range)	FHH OR FLL Event (FMPLL_0_CLK frequency out of range)
RGM_Fxx[7]	PMU	LVD 4.5	LVD 4.5
RGM_Fxx[8]	CFLASH0	Fatal Error	Fatal Error
	DFLASH0	Fatal Error	Fatal Error
	ECSM_0	ECC not correctable error	Not implemented
	ECSM_1	ECC not correctable error	Not implemented
RGM_Fxx[9]	FMPLL_1	Not implemented	Fail Event (Loss of lock)
RGM_Fxx[10]		Not implemented	Not implemented

Table 15. SPC560P50/SPC56AP60 functional reset source mapping comparison (continued)

Register bit	Module	SPC56AP60 reset source	SPC560P50 reset source
RGM_Fxx[11]	CMU_1	FHH OR FLL Event (SYS_CLK frequency out of range)	FHH OR FLL Event (MC_CLK frequency out of range)
RGM_Fxx[12:14]		Not implemented	Not implemented
RGM_Fxx[15]	Reset PAD(1)	External reset pin ($\overline{\text{RESET}}$)	External reset pin ($\overline{\text{RESET}}$)

1. RESET PAD on SPC56AP60 is pulled-down out of reset while on SPC560Pr0xx devices it is pulled-up out of reset

9 Power supplies

The SPC56AP60 device has a dedicated supply voltage (lower than product supply) to the external ballast which reduces power consumption.

This configuration decreases supply voltage to the BJT, allowing it to operate at a supply voltage as low as 1.9 V, whereas the PMU in the SoC still requires at least 2.6 V.

The configuration can be applied if the NPN transistor BC817su used has the following electrical features: $H_{fe} > 80$, $V_{CEsat} < 500$ mV for load currents up to 100 mA.

10 Debug interface

There is a Nexus Level 2+ debug interface on both SPC560P50 and SPC56AP60 devices.

Only on the SPC56AP60 device, a Nexus AXBS Slave Port Sniffer (NASP) is implemented for each SRAM port controller.

According to this, in order to assure the required bandwidth for debug opertations, on SPC56AP60 devices, 12 MDO pins are avalaible (on emulation package LQFP176), DDR support for Nexus is implemented and RDY is available as alternate function (not selected by default in order to assure the compatibility with SPC560P50 devices) on packages LQFP100 and LQFP144, and as dedicated pin on emulation package LQFP176.

Appendix A Additional information

A.1 Reference document

32-bit MCU family built on the Power Architecture™ embedded category for automotive chassis and safety electronics applications (RM0022, Doc ID 14891).

A.2 Acronyms

Table 16. Acronyms

Acronym	Name
ADC	Analog-to-digital converter
AUTOSAR	AUTomotive Open System ARchitecture
CRC	Cyclic redundancy check
CTU	Cross triggering unit
eDMA	Enhanced direct memory access
FCU	Fault collection unit
FCCU	Fault collection and control unit
MCU	Microcontroller unit
SIUL	System integration unit lite

Revision history

Table 17. Document revision history

Date	Revision	Changes
21-Jan-2011	1	Initial release
08-Sep-2011	2	In *Table 8: Application view on page 16*, changed “SPC560P40xF” to “SPC56AP60xF”

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